8-Channel 1.0-1.25 Gbps Transceiver

FEATURES

- Eight independent 1.0-1.25 Gbit/s transceivers
- Ultra low power operation: 1.25 Watts typical
- Integrated serializer/deserializer, clock synthesis, clock recovery, and 8B/10B encode/decode logic
- Physical Coding Sublayer (PCS) logic for Gigabit Ethernet
- Optional receive FIFO which synchronizes incoming data to local clock domain
- Dual Data Rate (DDR) parallel interface with clock forwarding to halve ASIC terminal count and simplify timing
- Extensive control of loopback, BIST, and operating modes via 802.3 compliant MDC/MDIO serial interface
- Built-in packet generator/checker
- "Trunking" feature to de-skew and align received parallel data across eight channels
- IEEE 1149.1 JTAG testing support
- IEEE 802.3z Gigabit Ethernet and ANSI X3T11 FibreChannel support
- High speed outputs which feature programmable output current to directly drive dual-terminated line
- 2.5 V, 0.25 µ CMOS technology with 3.3V tolerant I/O
- Direct interface to optical modules, coax, or serial backplanes
- Small footprint 19x19 mm, 289-pin PBGA

APPLICATIONS

- High speed serial backplanes
- Gigabit Ethernet links
- FibreChannel links
- Intra-system interconnect
- ASIC to PMD link

GENERAL DESCRIPTION

The OctalPHY™ is an octal PHYsical layer transceiver ideal for systems requiring large numbers of point-to-point gigabit links. It provides eight individual serial channels capable of operation at up to 1.25 Gbps, which may be grouped together to form a single 12.5 Gbps bidirectional link.

The OctalPHY includes 8B/10B block coding logic (compliant with 802.3z Gigabit Ethernet and FibreChannel requirements) which produces run length limited data streams for serial transmission.

A receive FIFO optionally aligns all incoming parallel data to the local clock domain, adding or removing IDLE sequences as required. This simplifies implementation of the upstream ASIC by removing the requirement to deal with multiple clock domains.

When trunking is enabled, the OctalPHY can remove cable skew differences equivalent to several meters, presenting 8-byte data vectors at the receive interface exactly as they were transmitted.

EXAMPLE ARCHITECTURE

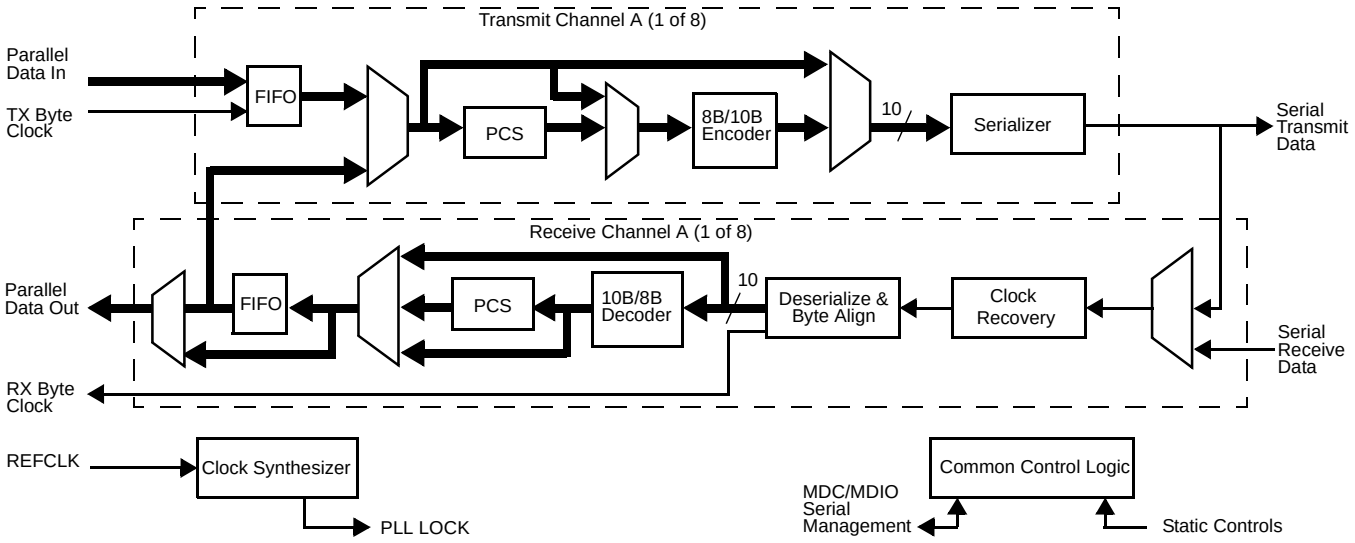
The first figure on the next page shows the OctalPHY in a switch application. This implementation uses eight channels of 1.25 Gbaud per linecard, requiring only 32 signal pins per linecard and 128 for the switch card, providing up to 32 Gbps total payload capacity to the switch fabric.

The 5-bit DDR interface of the OctalPHY saves pins on the switch device. An additional OctalPHY operated in trunking mode creates a cost effective 10 Gbps uplink, capable of directly driving copper or various optical transports.

The dotted lines in the figure depict the system clock domains. Note that even though the recovered clock from any or all serial links may be asynchronous to the local clock, the OctalPHY bridges these domains so that the switch fabric and linecards may be designed in only a single clock domain.

The OctalPHY creates a highly integrated and cost effective physical layer solution for Gigabit Ethernet or FibreChannel external interfaces.

BLOCK DIAGRAM



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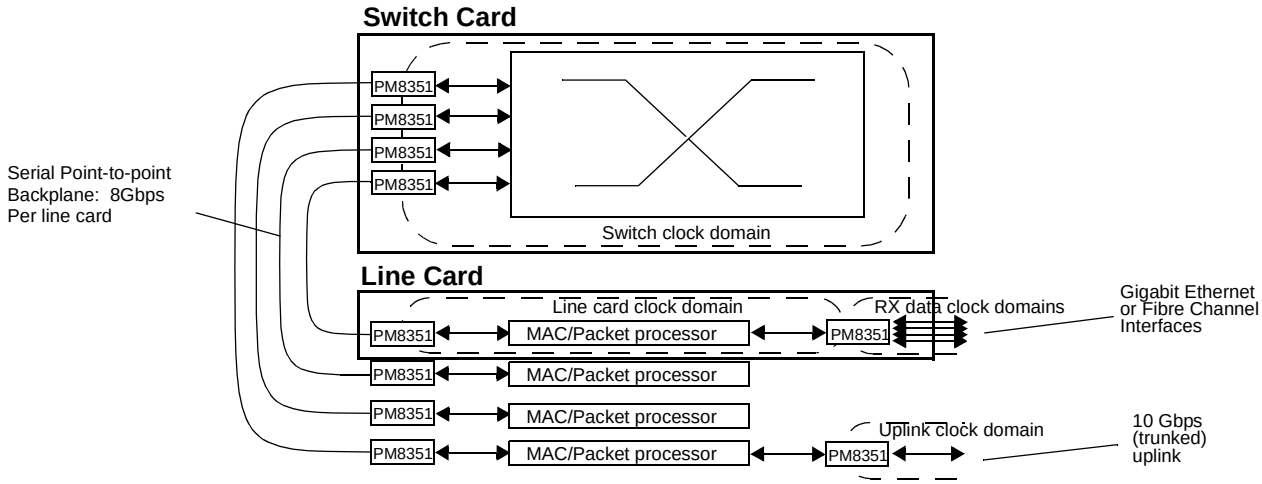
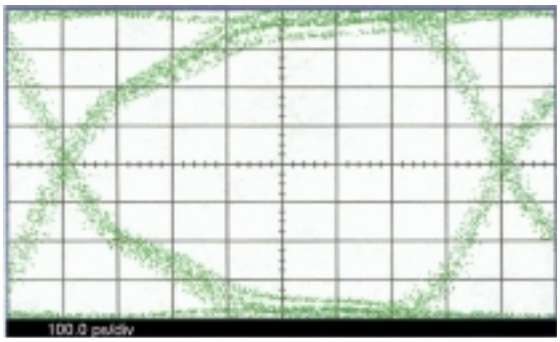
32 GBPS SWITCH APPLICATION



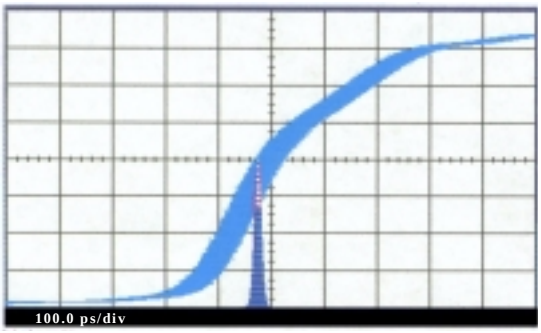
EYE DIAGRAM

Produced by the OctalPHY when driving a 50 Ohm cable, terminated at both near and far ends.



JITTER

Jitter histogram of the OctalPHY showing 6.8 picoseconds, 1 σ jitter with all channels operating.



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