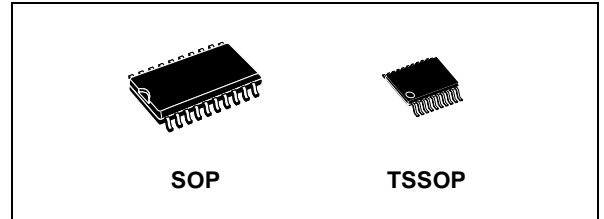




# 74VHCT574A

## OCTAL D-TYPE FLIP FLOP WITH 3 STATE OUTPUTS NON INVERTING

- HIGH SPEED:  
 $f_{MAX} = 180 \text{ MHz (TYP.) at } V_{CC} = 5\text{V}$
- LOW POWER DISSIPATION:  
 $I_{CC} = 4 \mu\text{A (MAX.) at } T_A = 25^\circ\text{C}$
- COMPATIBLE WITH TTL OUTPUTS:  
 $V_{IH} = 2\text{V (MIN.)}, V_{IL} = 0.8\text{V (MAX)}$
- POWER DOWN PROTECTION ON INPUTS & OUTPUTS
- SYMMETRICAL OUTPUT IMPEDANCE:  
 $|I_{OH}| = I_{OL} = 8 \text{ mA (MIN)}$
- BALANCED PROPAGATION DELAYS:  
 $t_{PLH} \cong t_{PHL}$
- OPERATING VOLTAGE RANGE:  
 $V_{CC(OPR)} = 4.5\text{V to } 5.5\text{V}$
- PIN AND FUNCTION COMPATIBLE WITH 74 SERIES 574
- IMPROVED LATCH-UP IMMUNITY
- LOW NOISE:  $V_{OLP} = 0.9\text{V (MAX.)}$



**Table 1: Order Codes**

PACKAGE	T & R
SOP	74VHCT574AMTR
TSSOP	74VHCT574ATTR

### DESCRIPTION

The 74VHCT574A is an advanced high-speed CMOS OCTAL D-TYPE FLIP FLOP with 3 STATE OUTPUTS NON INVERTING fabricated with sub-micron silicon gate and double-layer metal wiring C<sup>2</sup>MOS technology.

These 8 bit D-Type flip-flop is controlled by a clock input (CK) and an output enable input ( $\overline{OE}$ ).

On the positive transition of the clock, the Q outputs will be set to the logic states that were setup at the D inputs.

When the ( $\overline{OE}$ ) input is low, the 8 outputs will be in a normal logic state (high or low logic level) and when ( $\overline{OE}$ ) is high, the outputs will be in a high impedance state.

The Output control does not affect the internal operation of flip flop; that is, the old data can be retained or the new data can be entered even while the outputs are off.

Power down protection is provided on all inputs and outputs and 0 to 7V can be accepted on inputs with no regard to the supply voltage. This device can be used to interface 5V to 3V since all inputs are equipped with TTL threshold.

All inputs and outputs are equipped with protection circuits against static discharge, giving them 2KV ESD immunity and transient excess voltage.

**Figure 1: Pin Connection And IEC Logic Symbols**

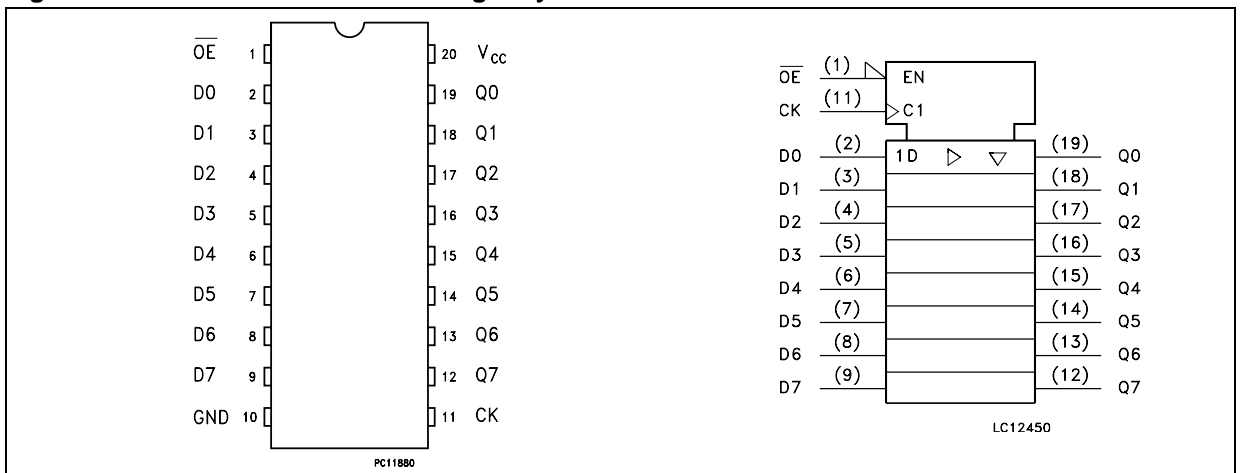


Figure 2: Input Equivalent Circuit

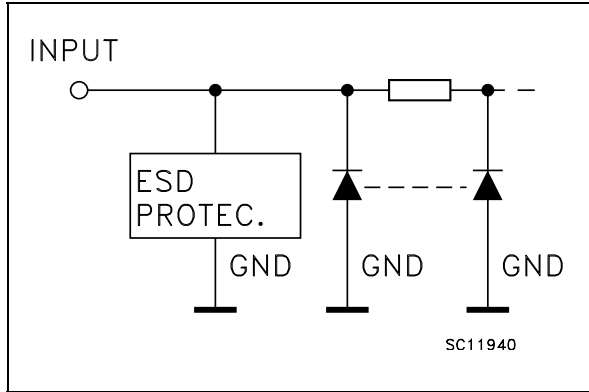


Table 2: Pin Description

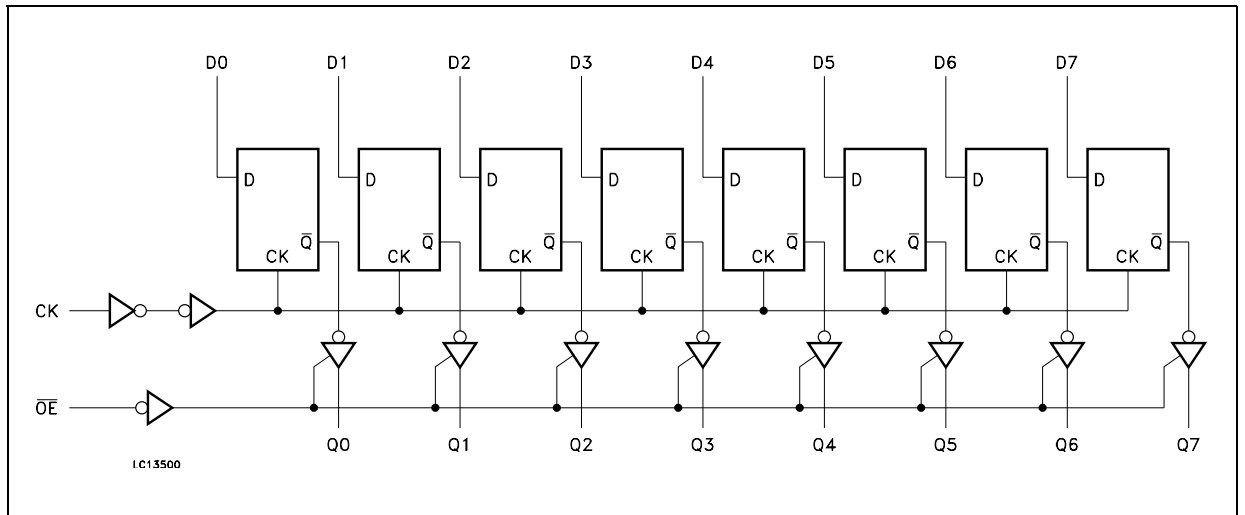
PIN N°	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}$	3-State Output Enable Input (Active LOW)
2, 3, 4, 5, 6, 7, 8, 9	D0 to D7	Data Inputs
12, 13, 14, 15, 16, 17, 18, 19	Q0 to Q7	3-State Outputs
11	CK	Clock Input (LOW-to-HIGH Edge Triggered)
10	GND	Ground (0V)
20	V <sub>CC</sub>	Positive Supply Voltage

Table 3: Truth Table

INPUTS			OUTPUT
$\overline{OE}$	CK	D	Q
H	X	X	Z
L		X	NO CHANGE
L		L	L
L		H	H

X : Don't Care  
Z : High Impedance

Figure 3: Logic Diagram



**Table 4: Absolute Maximum Ratings**

Symbol	Parameter	Value	Unit
$V_{CC}$	Supply Voltage	-0.5 to +7.0	V
$V_I$	DC Input Voltage	-0.5 to +7.0	V
$V_O$	DC Output Voltage (see note 1)	-0.5 to +7.0	V
$V_O$	DC Output Voltage (see note 2)	-0.5 to $V_{CC} + 0.5$	V
$I_{IK}$	DC Input Diode Current	- 20	mA
$I_{OK}$	DC Output Diode Current	$\pm 20$	mA
$I_O$	DC Output Current	$\pm 25$	mA
$I_{CC}$ or $I_{GND}$	DC $V_{CC}$ or Ground Current	$\pm 50$	mA
$T_{stg}$	Storage Temperature	-65 to +150	°C
$T_L$	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied

- 1) Output in OFF State  
2) High or Low State

**Table 5: Recommended Operating Conditions**

Symbol	Parameter	Value	Unit
$V_{CC}$	Supply Voltage	4.5 to 5.5	V
$V_I$	Input Voltage	0 to 5.5	V
$V_O$	Output Voltage (see note 1)	0 to 5.5	V
$V_O$	Output Voltage (see note 2)	0 to $V_{CC}$	V
$T_{op}$	Operating Temperature	-55 to 125	°C
dt/dv	Input Rise and Fall Time (see note 3) ( $V_{CC} = 5.0 \pm 0.5V$ )	0 to 20	ns/V

- 1) Output in OFF State  
2) High or Low State  
3)  $V_{IN}$  from 0.8V to 2V

Table 6: DC Specifications

Symbol	Parameter	Test Condition		Value						Unit	
		V <sub>CC</sub> (V)		T <sub>A</sub> = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
V <sub>IH</sub>	High Level Input Voltage	4.5 to 5.5		2			2		2		V
V <sub>IL</sub>	Low Level Input Voltage	4.5 to 5.5				0.8		0.8		0.8	V
V <sub>OH</sub>	High Level Output Voltage	4.5	I <sub>O</sub> =-50 μA	4.4	4.5		4.4		4.4		V
		4.5	I <sub>O</sub> =-8 mA	3.94			3.8		3.7		
V <sub>OL</sub>	Low Level Output Voltage	4.5	I <sub>O</sub> =50 μA		0.0	0.1		0.1		0.1	V
		4.5	I <sub>O</sub> =8 mA			0.36		0.44		0.55	
I <sub>OZ</sub>	High Impedance Output Leakage Current	4.5 to 5.5	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> V <sub>O</sub> = 0V to 5.5V			±0.25		± 2.5		± 2.5	μA
I <sub>I</sub>	Input Leakage Current	0 to 5.5	V <sub>I</sub> = 5.5V or GND			± 0.1		± 1.0		± 1.0	μA
I <sub>CC</sub>	Quiescent Supply Current	5.5	V <sub>I</sub> = V <sub>CC</sub> or GND			4		40		40	μA
+I <sub>CC</sub>	Additional Worst Case Supply Current	5.5	One Input at 3.4V, other input at V <sub>CC</sub> or GND			1.35		1.5		1.5	mA
I <sub>OPD</sub>	Output Leakage Current	0	V <sub>OUT</sub> = 5.5V			0.5		5.0		5.0	μA

Table 7: AC Electrical Characteristics (Input t<sub>r</sub> = t<sub>f</sub> = 3ns)

Symbol	Parameter	Test Condition		Value						Unit	
		V <sub>CC</sub> (V)	C <sub>L</sub> (pF)	T <sub>A</sub> = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Time CK to Q	5.0(*)	15		5.5	8.6	1.0	10.0	1.0	10.0	ns
		5.0(*)	50		7.0	10.6	1.0	12.0	1.0	12.0	
t <sub>PZL</sub> t <sub>PZH</sub>	Output Enable Time	5.0(*)	15	RL = 1KΩ	5.0	9.0	1.0	10.5	1.0	10.5	ns
		5.0(*)	50		6.0	11.0	1.0	12.5	1.0	12.5	
t <sub>PLZ</sub> t <sub>PHZ</sub>	Output Disable Time	5.0(*)	50	RL = 1KΩ	7.0	10.1	1.0	11.5	1.0	11.5	ns
f <sub>MAX</sub>	Maximum Clock Frequency	5.0(*)	15		90	140		80		80	MHz
		5.0(*)	50		85	130					
t <sub>OSLH</sub> t <sub>OSHL</sub>	Output to Output Skew time (note 1)	5.0(*)	50			1.5		1.5		1.5	ns

(\*) Voltage range is 5.0V ± 0.5V

Note 1: Parameter guaranteed by design. t<sub>soLH</sub> = |t<sub>pLHm</sub> - t<sub>pLHn</sub>|, t<sub>soHL</sub> = |t<sub>pHLm</sub> - t<sub>pHLn</sub>|

Table 8: Capacitive Characteristics

Symbol	Parameter	Test Condition		Value						Unit
				T <sub>A</sub> = 25°C			-40 to 85°C		-55 to 125°C	
		Min.	Typ.	Max.	Min.	Max.	Min.	Max.		
C <sub>IN</sub>	Input Capacitance		4	10		10		10	pF	
C <sub>OUT</sub>	Output Capacitance		9						pF	
C <sub>PD</sub>	Power Dissipation Capacitance (note 1)		25						pF	

1) C<sub>PD</sub> is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation.  $I_{CC(oper)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/8$  (per Flip-Flop)

Table 9: Dynamic Switching Characteristics

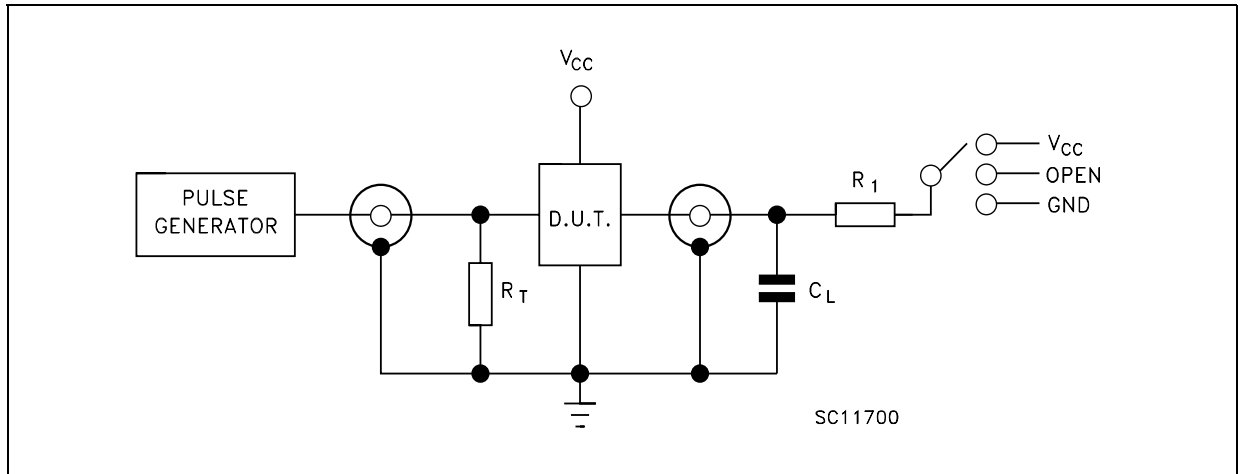
Symbol	Parameter	Test Condition		Value						Unit	
				T <sub>A</sub> = 25°C			-40 to 85°C		-55 to 125°C		
		V <sub>CC</sub> (V)		Min.	Typ.	Max.	Min.	Max.	Min.		Max.
V <sub>OLP</sub>	Dynamic Low Voltage Quiet Output (note 1, 2)	5.0	C <sub>L</sub> = 50 pF		1.2	1.6					V
V <sub>OLV</sub>				-1.6	-1.2						
V <sub>IHD</sub>	Dynamic High Voltage Input (note 1, 3)				3.5						
V <sub>ILD</sub>	Dynamic Low Voltage Input (note 1, 3)						1.5				

1) Worst case package.

2) Max number of outputs defined as (n). Data inputs are driven 0V to 3.0V, (n-1) outputs switching and one output at GND.

3) Max number of data inputs (n) switching. (n-1) switching 0V to 3.0V. Inputs under test switching: 3.0V to threshold (V<sub>ILD</sub>), 0V to threshold (V<sub>IHD</sub>), f=1MHz.

Figure 4: Test Circuit



TEST	SWITCH
$t_{PLH}, t_{PHL}$	Open
$t_{PZL}, t_{PLZ}$	$V_{CC}$
$t_{PZH}, t_{PHZ}$	GND

$C_L = 15/50\text{pF}$  or equivalent (includes jig and probe capacitance)

$R_L = R_1 = 1\text{K}\Omega$  or equivalent

$R_T = Z_{OUT}$  of pulse generator (typically  $50\Omega$ )

Figure 5: Waveform - Propagation Delays, Setup And Hold Times ( $f=1\text{MHz}$ ; 50% duty cycle)

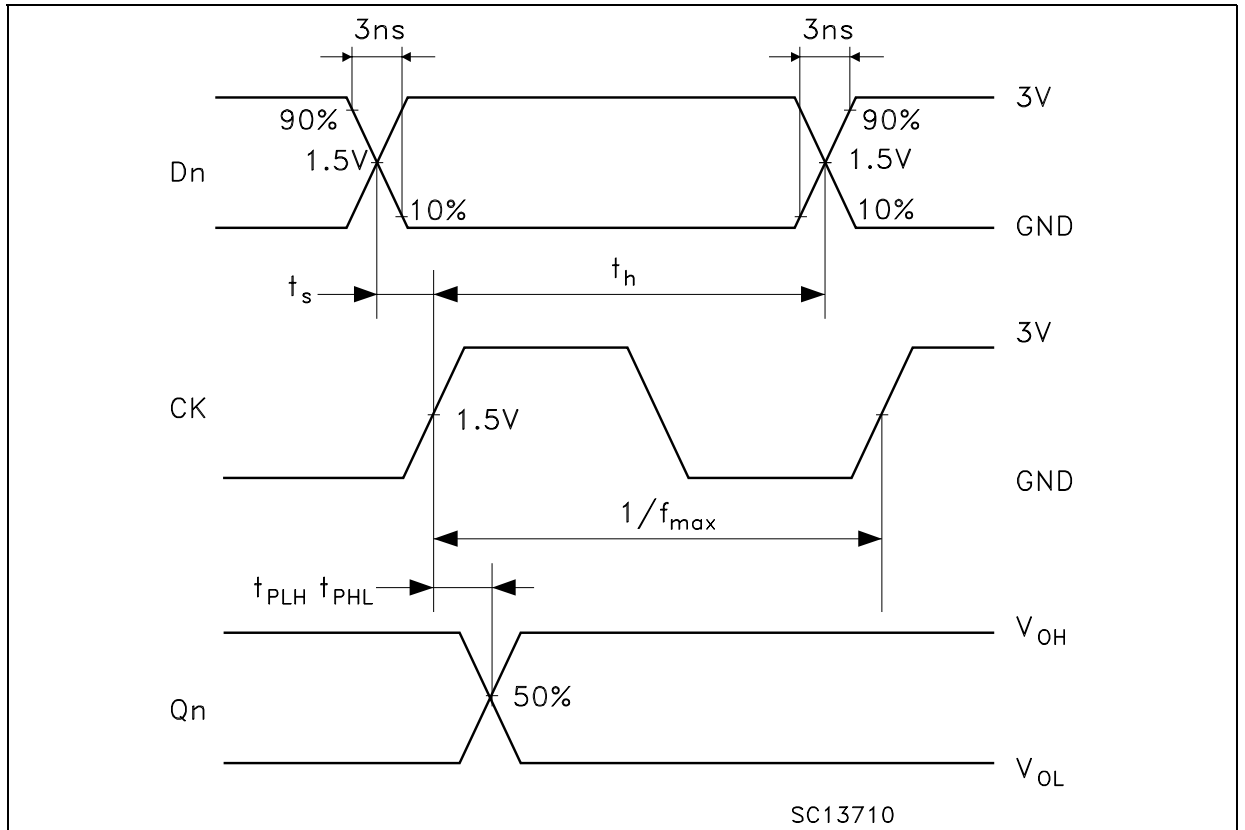
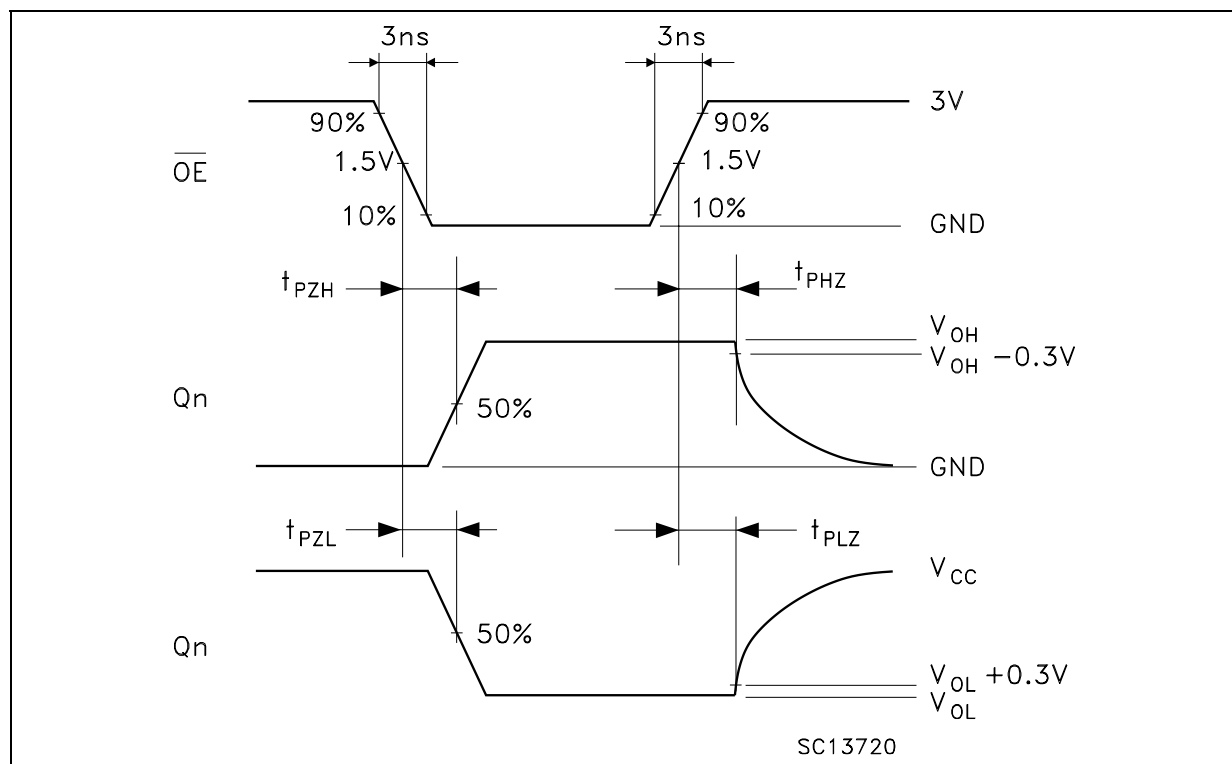
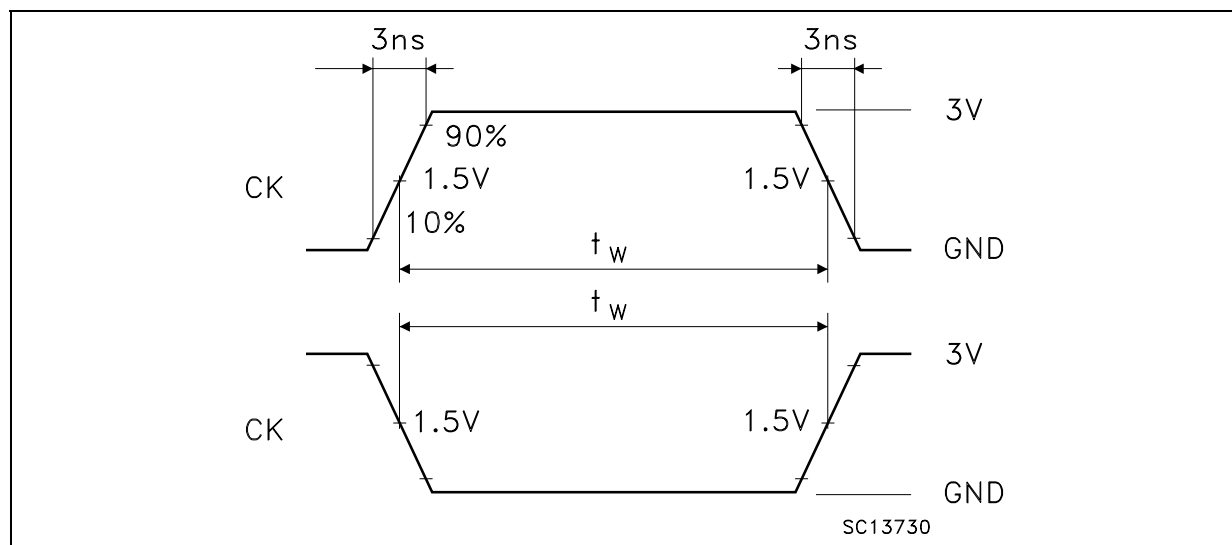
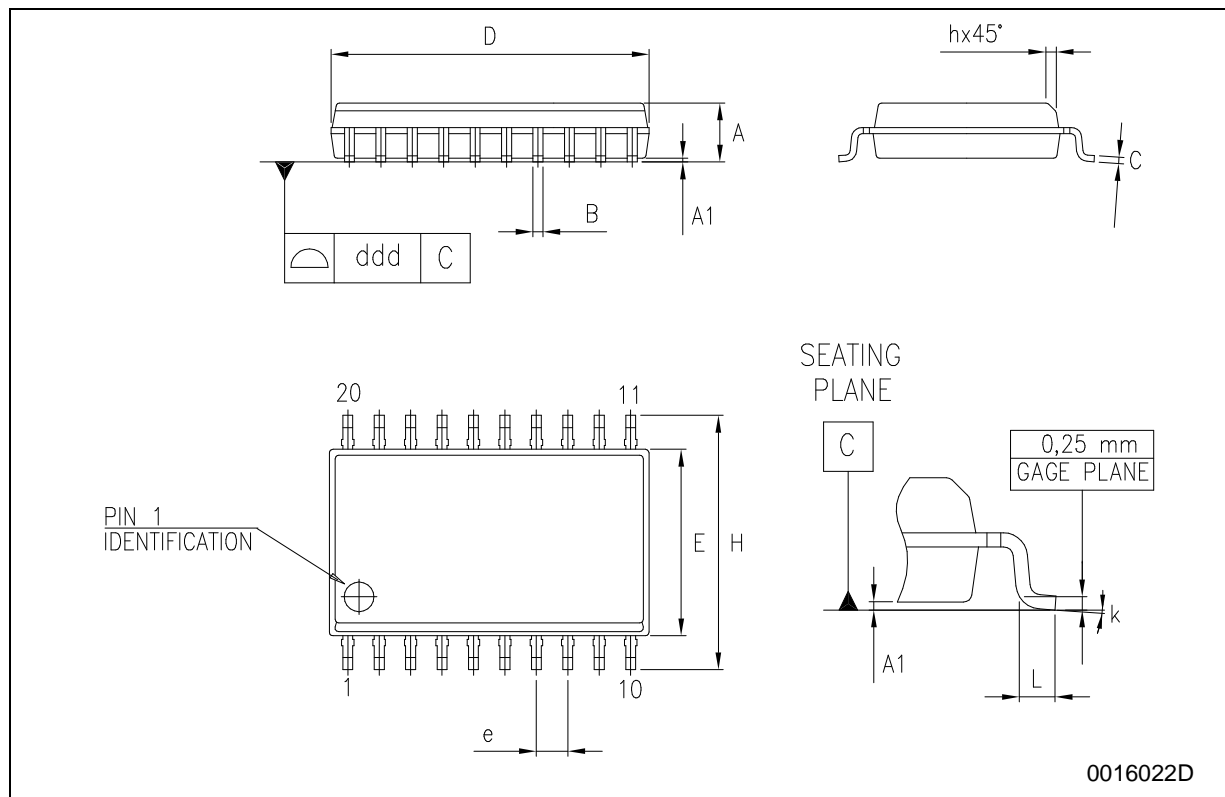


Figure 6: Waveform - Output Enable And Disable Times ( $f=1\text{MHz}$ ; 50% duty cycle)Figure 7: Waveform - Pulse Width ( $f=1\text{MHz}$ ; 50% duty cycle)

## SO-20 MECHANICAL DATA

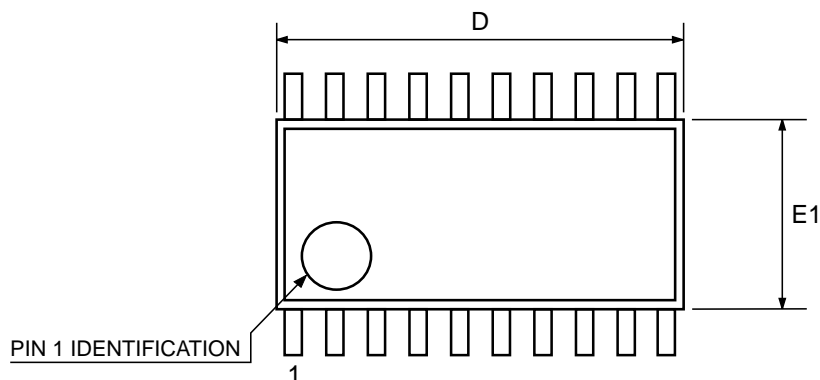
DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.35		2.65	0.093		0.104
A1	0.1		0.30	0.004		0.012
B	0.33		0.51	0.013		0.020
C	0.23		0.32	0.009		0.013
D	12.60		13.00	0.496		0.512
E	7.4		7.6	0.291		0.299
e		1.27			0.050	
H	10.00		10.65	0.394		0.419
h	0.25		0.75	0.010		0.030
L	0.4		1.27	0.016		0.050
k	0°		8°	0°		8°
ddd			0.100			0.004





## TSSOP20 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.2			0.047
A1	0.05		0.15	0.002	0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0079
D	6.4	6.5	6.6	0.252	0.256	0.260
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030



0087225C

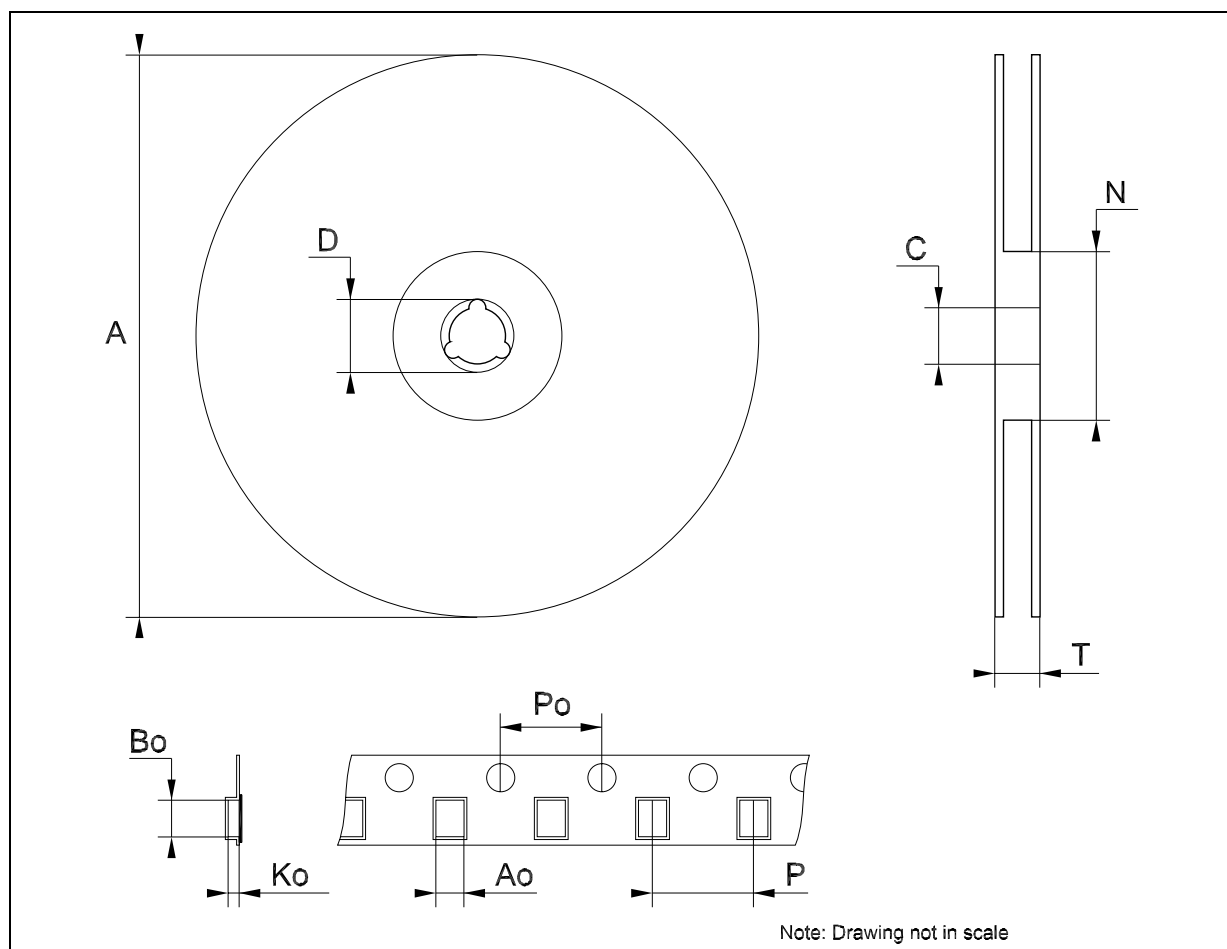
## Tape &amp; Reel SO-20 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			30.4			1.197
Ao	10.8		11	0.425		0.433
Bo	13.2		13.4	0.520		0.528
Ko	3.1		3.3	0.122		0.130
Po	3.9		4.1	0.153		0.161
P	11.9		12.1	0.468		0.476



### Tape & Reel TSSOP20 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			22.4			0.882
Ao	6.8		7	0.268		0.276
Bo	6.9		7.1	0.272		0.280
Ko	1.7		1.9	0.067		0.075
Po	3.9		4.1	0.153		0.161
P	11.9		12.1	0.468		0.476



**Table 10: Revision History**

<b>Date</b>	<b>Revision</b>	<b>Description of Changes</b>
16-Dec-2004	4	Order Codes Revision - pag. 1.

Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

The ST logo is a registered trademark of STMicroelectronics

All other names are the property of their respective owners

© 2004 STMicroelectronics - All Rights Reserved

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

[www.st.com](http://www.st.com)