

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

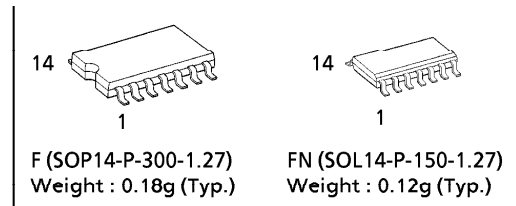
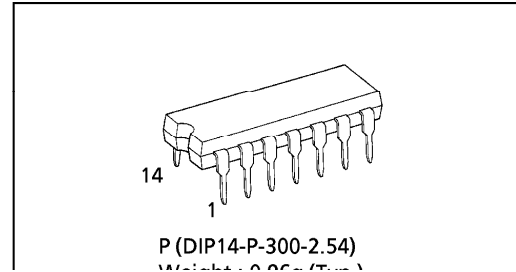
# TC4013BP, TC4013BF, TC4013BFN

## TC4013B DUAL D-TYPE FLIP-FLOP

TC4013B contains two independent circuits of D type flip-flop. The input level applied to DATA input are transferred to Q and  $\bar{Q}$  output by rising edge of the clock pulse. When SET input is placed at "H", and RESET input is placed at "L", outputs become Q = "H", and  $\bar{Q}$  = "L". When RESET input is placed at "H", and SET input is placed at "L", outputs become Q = "L" and  $\bar{Q}$  = "H". When both of RESET input

= "H".

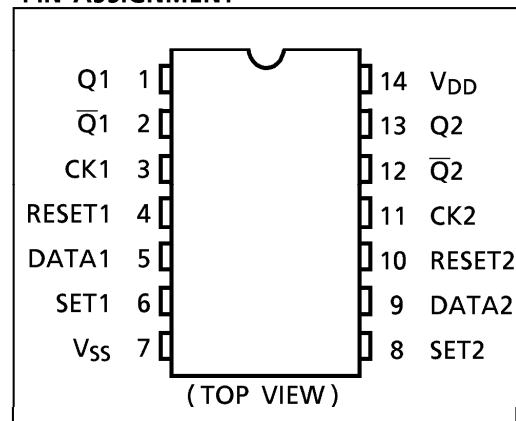
(Note) The JEDEC SOP (FN) is not available in Japan.



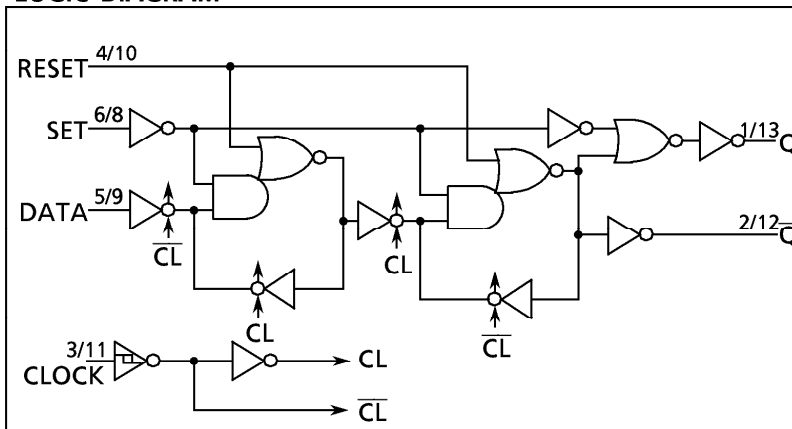
### MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	$V_{DD}$	$V_{SS} - 0.5 \sim V_{SS} + 20$	V
Input Voltage	$V_{IN}$	$V_{SS} - 0.5 \sim V_{DD} + 0.5$	V
Output Voltage	$V_{OUT}$	$V_{SS} - 0.5 \sim V_{DD} + 0.5$	V
DC Input Current	$I_{IN}$	$\pm 10$	mA
Power Dissipation	$P_D$	300 (DIP) / 180 (SOIC)	mW
Operating Temperature Range	$T_{opr}$	-40~85	°C
Storage Temperature Range	$T_{stg}$	-65~150	°C

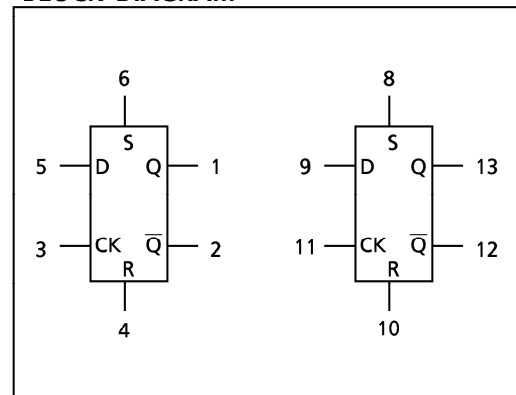
### PIN ASSIGNMENT



### LOGIC DIAGRAM






### BLOCK DIAGRAM



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**TRUTH TABLE**

INPUTS				OUTPUTS	
RESET	SET	DATA	CK $\Delta$	Q <sub>n+1</sub>	$\overline{Q}_{n+1}$
L	H	*	*	H	L
H	L	*	*	L	H
H	H	*	*	H	H
L	L	L		L	H
L	L	H		H	L
L	L	*		Q <sub>n</sub> $\cdot$	$\overline{Q}_n\cdot$

\* : Don't Care  
 $\Delta$  : Level Change  
 $\cdot$  : No Change

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- The information contained herein is subject to change without notice.

RECOMMENDED OPERATING CONDITIONS ( $V_{SS} = 0V$ )

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
DC Supply Voltage	$V_{DD}$		3	—	18	V
Input Voltage	$V_{IN}$		0	—	$V_{DD}$	V

STATIC ELECTRICAL CHARACTERISTICS ( $V_{SS} = 0V$ )

CHARACTERISTIC	SYM-BOL	TEST CONDITION	$V_{DD}$ (V)	-40°C		25°C			85°C		UNIT	
				MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.		
High-Level Output Voltage	$V_{OH}$	$ I_{OUT}  < 1\mu A$ $V_{IN} = V_{SS}, V_{DD}$	5	4.95	—	4.95	5.00	—	4.95	—	V	
			10	9.95	—	9.95	10.00	—	9.95	—		
			15	14.95	—	14.95	15.00	—	14.95	—		
Low-Level Output Voltage	$V_{OL}$	$ I_{OUT}  < 1\mu A$ $V_{IN} = V_{SS}, V_{DD}$	5	—	0.05	—	0.00	0.05	—	0.05	V	
			10	—	0.05	—	0.00	0.05	—	0.05		
			15	—	0.05	—	0.00	0.05	—	0.05		
Output High Current	$I_{OH}$	$V_{OH} = 4.6V$ $V_{OH} = 2.5V$ $V_{OH} = 9.5V$ $V_{OH} = 13.5V$ $V_{IN} = V_{SS}, V_{DD}$	5	-0.61	—	-0.51	-1.0	—	-0.42	—	mA	
			5	-2.50	—	-2.10	-4.0	—	-1.70	—		
			10	-1.50	—	-1.30	-2.2	—	-1.10	—		
			15	-4.00	—	-3.40	-9.0	—	-2.80	—		
Output Low Current	$I_{OL}$	$V_{OL} = 0.4V$ $V_{OL} = 0.5V$ $V_{OL} = 1.5V$ $V_{IN} = V_{SS}, V_{DD}$	5	0.61	—	0.51	1.2	—	0.42	—	mA	
			10	1.50	—	1.30	3.2	—	1.10	—		
			15	4.00	—	3.40	12.0	—	2.80	—		
Input High Voltage	$V_{IH}$	$V_{OUT} = 0.5V, 4.5V$ $V_{OUT} = 1.0V, 9.0V$ $V_{OUT} = 1.5V, 13.5V$ $ I_{OUT}  < 1\mu A$	5	3.5	—	3.5	2.75	—	3.50	—	V	
			10	7.0	—	7.0	5.50	—	7.00	—		
			15	11.0	—	11.0	8.25	—	11.00	—		
Input Low Voltage	$V_{IL}$	$V_{OUT} = 0.5V, 4.5V$ $V_{OUT} = 1.0V, 9.0V$ $V_{OUT} = 1.5V, 13.5V$ $ I_{OUT}  < 1\mu A$	5	—	1.5	—	2.25	1.5	—	1.5	V	
			10	—	3.0	—	4.50	3.0	—	3.0		
			15	—	4.0	—	6.75	4.0	—	4.0		
Input Current	"H" Level	$I_{IH}$	$V_{IH} = 18V$	18	—	0.1	—	$10^{-5}$	0.1	—	1.0	μA
	"L" Level	$I_{IL}$	$V_{IL} = 0V$	18	—	-0.1	—	$-10^{-5}$	-0.1	—	-1.0	
Quiescent Supply Current	$I_{DD}$	$V_{IN} = V_{SS}, V_{DD} *$	5	—	1	—	0.002	1	—	30	μA	
			10	—	2	—	0.004	2	—	60		
			15	—	4	—	0.008	4	—	120		

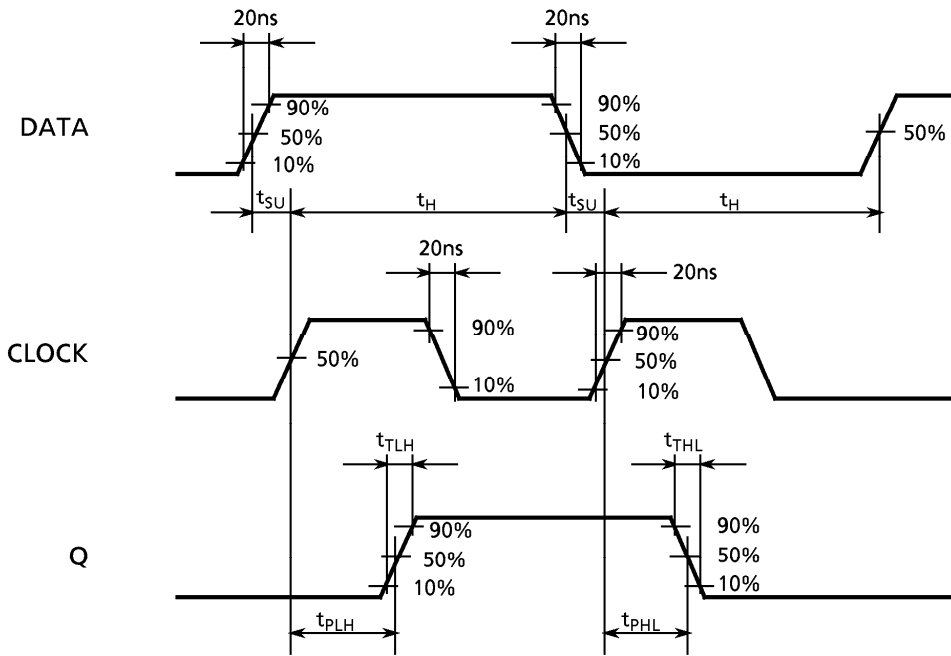
\* All valid input combinations.

## DYNAMIC ELECTRICAL CHARACTERISTICS (Ta = 25°C, Vss = 0V, CL = 50pF)

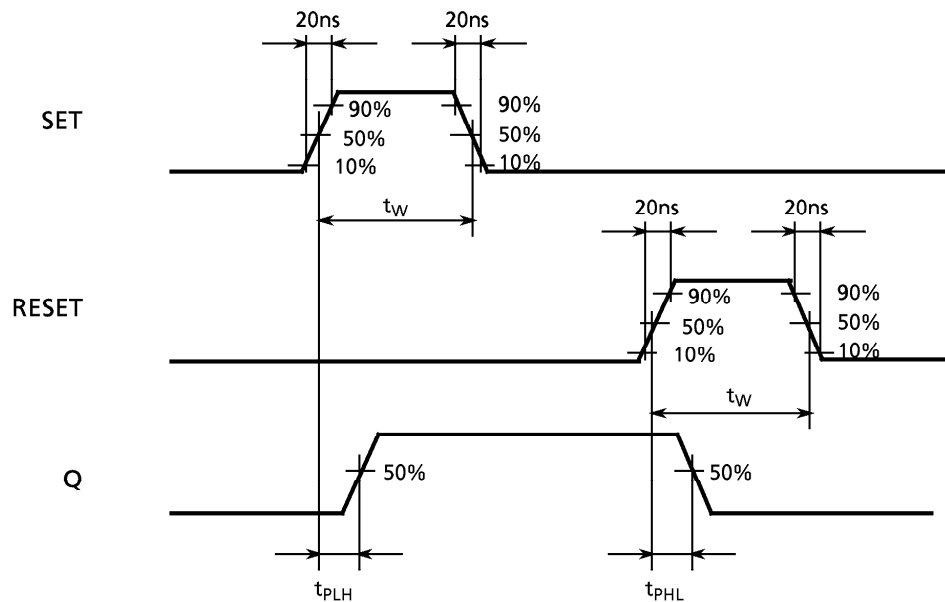
CHARACTERISTIC	SYMBOL	TEST CONDITION	V <sub>DD</sub> (V)	MIN.	TYP.	MAX.	UNIT
Output Transition Time (Low to High)	t <sub>TLH</sub>		5	—	70	200	ns
			10	—	35	100	
			15	—	30	80	
Output Transition Time (High to Low)	t <sub>THL</sub>		5	—	70	200	
			10	—	35	100	
			15	—	30	80	
Propagation Delay Time (CK - Q, $\bar{Q}$ )	t <sub>pLH</sub> t <sub>pHL</sub>		5	—	130	300	
			10	—	65	130	
			15	—	50	90	
Propagation Delay Time (SET, RESET - Q, $\bar{Q}$ )	t <sub>pLH</sub>		5	—	110	300	
			10	—	50	130	
			15	—	40	90	
Propagation Delay Time (SET, RESET - Q, $\bar{Q}$ )	t <sub>pHL</sub>		5	—	110	300	
			10	—	50	130	
			15	—	40	90	
Max. Clock Frequency	f <sub>CL</sub>		5	3.5	8	—	MHz
			10	8.0	16	—	
			15	12.0	20	—	
Max. Clock Input Rise Time Max. Clock Input Fall Time	t <sub>rCL</sub> t <sub>fCL</sub>		5	No Limit			μs
			10				
			15				
Min. Pulse Width (SET, RESET)	t <sub>w</sub>		5	—	60	180	ns
			10	—	30	80	
			15	—	25	50	
Min. Clock Pulse Width	t <sub>w</sub>		5	—	60	140	
			10	—	30	60	
			15	—	25	40	
Min. Set-up Time (DATA - CK)	t <sub>su</sub>		5	—	—	40	ns
			10	—	—	20	
			15	—	—	15	
Min. Hold Time (DATA - CK)	t <sub>H</sub>		5	—	20	40	
			10	—	10	20	
			15	—	6	15	
Min. Removal Time (SET, RESET - CK)	t <sub>rem</sub>		5	—	—	40	
			10	—	—	20	
			15	—	—	15	
Input Capacitance	C <sub>IN</sub>			—	5	7.5	pF

WAVEFORM FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS

WAVEFORM 1

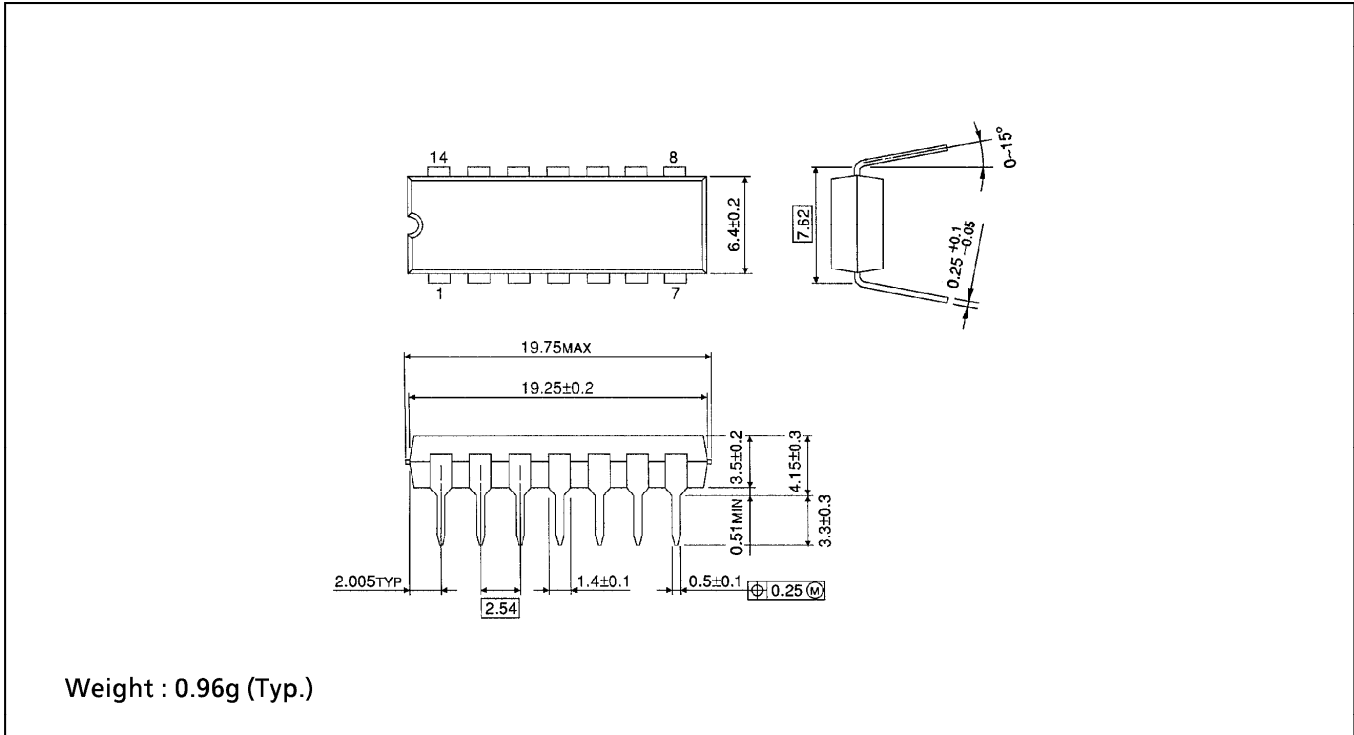


WAVEFORM 2



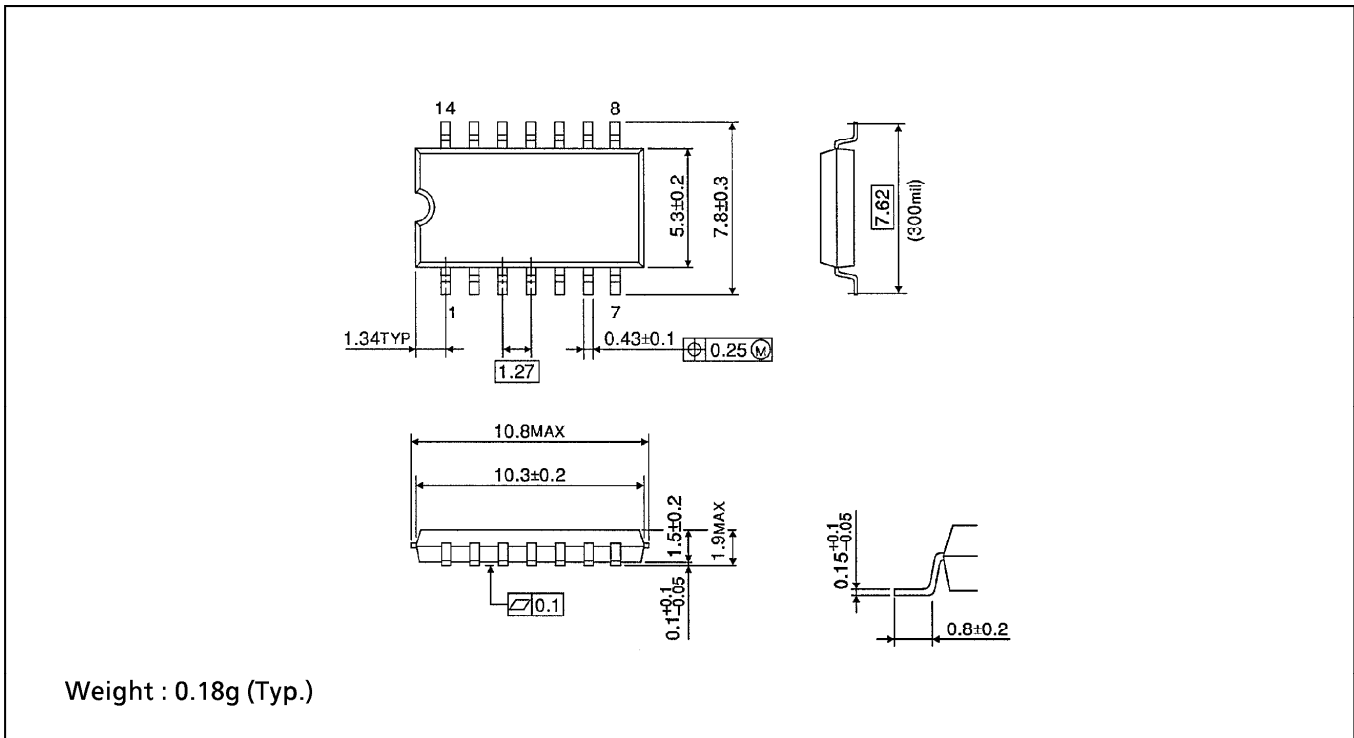
**DIP 14PIN OUTLINE DRAWING (DIP14-P-300-2.54)**

Unit in mm



**SOP 14PIN (200mil BODY) OUTLINE DRAWING (SOP14-P-300-1.27)**

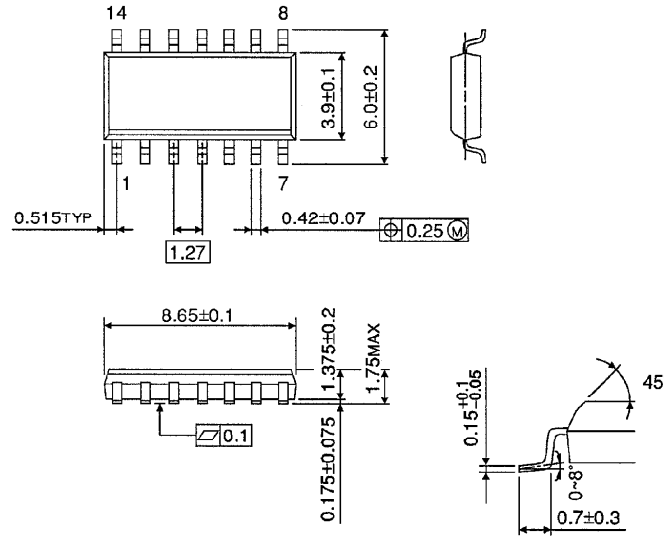
Unit in mm



**SOP 14PIN (150mil BODY) OUTLINE DRAWING (SOL14-P-150-1.27)**

Unit in mm

(Note) This package is not available in Japan.



Weight : 0.12g (Typ.)