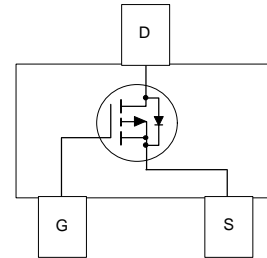
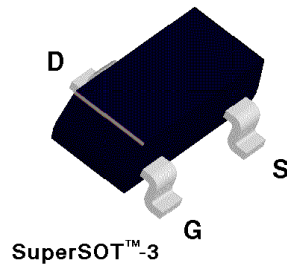


General Description

These P-Channel logic level enhancement mode power field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage applications such as notebook computer power management, portable electronics, and other battery powered circuits where fast high-side switching, and low in-line power loss are needed in a very small outline surface mount package.

Features

- -0.9 A, -30 V. $R_{DS(ON)} = 0.5 \Omega @ V_{GS} = -4.5 V$
 $R_{DS(ON)} = 0.3 \Omega @ V_{GS} = -10 V.$
- Industry standard outline SOT-23 surface mount package using proprietary SuperSOT™-3 design for superior thermal and electrical capabilities.
- High density cell design for extremely low $R_{DS(ON)}$.
- Exceptional on-resistance and maximum DC current capability.



Absolute Maximum Ratings

$T_A = 25^\circ C$ unless otherwise noted

Symbol	Parameter	NDS352AP	Units
V_{DSS}	Drain-Source Voltage	-30	V
V_{GSS}	Gate-Source Voltage - Continuous	±20	V
I_D	Maximum Drain Current - Continuous (Note 1a)	±0.9	A
	- Pulsed	±10	
P_D	Maximum Power Dissipation (Note 1a) (Note 1b)	0.5	W
		0.46	
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to 150	°C
THERMAL CHARACTERISTICS			
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	250	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	75	°C/W



Electrical Characteristics (T _A = 25°C unless otherwise noted)						
Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} = 0 V, I _D = -250 μA	-30			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = -24 V, V _{GS} = 0 V			-1	μA
			T _J = 125°C			-10
I _{GSSF}	Gate - Body Leakage, Forward	V _{GS} = 20 V, V _{DS} = 0 V			100	nA
I _{GSSR}	Gate - Body Leakage, Reverse	V _{GS} = -20 V, V _{DS} = 0 V			-100	nA
ON CHARACTERISTICS (Note 2)						
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = -250 μA	-0.8	-1.7	-2.5	V
			T _J = 125°C	-0.5	-1.4	
R _{DS(on)}	Static Drain-Source On-Resistance	V _{GS} = -4.5 V, I _D = -0.9 A		0.45	0.5	Ω
			T _J = 125°C		0.65	
		V _{GS} = -10 V, I _D = -1 A		0.25	0.3	
I _{D(on)}	On-State Drain Current	V _{GS} = -4.5 V, V _{DS} = -5 V	-2			A
g _{FS}	Forward Transconductance	V _{DS} = -5 V, I _D = -0.9 A		1.9		S
DYNAMIC CHARACTERISTICS						
C _{iss}	Input Capacitance	V _{DS} = -15 V, V _{GS} = 0 V, f = 1.0 MHz		135		pF
C _{oss}	Output Capacitance			88		pF
C _{rss}	Reverse Transfer Capacitance			40		pF
SWITCHING CHARACTERISTICS (Note 2)						
t _{d(on)}	Turn - On Delay Time	V _{DD} = -6 V, I _D = -1 A, V _{GS} = -4.5 V, R _{GEN} = 6 Ω		5	10	ns
t _r	Turn - On Rise Time			17	30	
t _{d(off)}	Turn - Off Delay Time			35	70	
t _f	Turn - Off Fall Time			30	60	
t _{d(on)}	Turn - On Delay Time	V _{DD} = -10 V, I _D = -1 A, V _{GS} = -10 V, R _{GEN} = 50 Ω		8	15	ns
t _r	Turn - On Rise Time			16	30	
t _{d(off)}	Turn - Off Delay Time			35	90	
t _f	Turn - Off Fall Time			30	90	
Q _g	Total Gate Charge	V _{DS} = -10 V, I _D = -0.9 A, V _{GS} = -4.5 V		2	3	nC
Q _{gs}	Gate-Source Charge			0.5		
Q _{gd}	Gate-Drain Charge			1		

Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuous Source Current				-0.42	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current				-10	A
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = -0.42$ (Note 2)		-0.8	-1.2	V

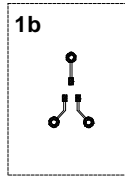
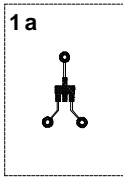
Notes:

- $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

$$P_D(t) = \frac{T_J - T_A}{R_{\theta JA}(t)} = \frac{T_J - T_A}{R_{\theta JC} + R_{\theta CA}(t)} = I_D^2(t) \times R_{DS(ON)} @ T_J$$

Typical $R_{\theta JA}$ using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

- 250°C/W when mounted on a 0.02 in² pad of 2oz copper.
- 270°C/W when mounted on a 0.001 in² pad of 2oz copper.



Scale 1 : 1 on letter size paper

- Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2.0\%$.