

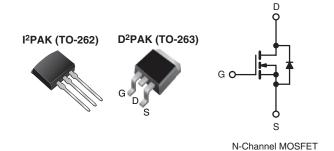
Vishay Siliconix

Reel RoHS

COMPLIANT

Power MOSFET

PRODUCT SUMMARY					
V _{DS} (V)	900				
R _{DS(on)} (Ω)	V _{GS} = 10 V 8.0				
Q _g (Max.) (nC)	38				
Q _{gs} (nC)	4.7				
Q _{gd} (nC)	21				
Configuration	Single				



FEATURES

- Surface Mount (IRFBF20S/SiHFBF20S)
- Low-Profile Through-Hole (IRFBF20L/SiHFBF20L)
- Available in Tape and (IRFBF20S/SiHFBF20S)
- Dynamic dV/dt Rating
- 150 °C Operating Temperature
- Fast Switching
- Fully Avalanche Rated
- Lead (Pb)-free Available

DESCRIPTION

Third generation Power MOSFETs form Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The D²PAK is a surface mount power package capabel of the accommodating die sizes up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface mount package. The D²PAK is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0 W in a typical surface mount application. The through-hole version (IRFBF20L/SiHFBF20L) is available for low-profile applications.

ORDERING INFORMATION						
Package	D ² PAK (TO-263)	D ² PAK (TO-263)	D ² PAK (TO-263)	I ² PAK (TO-262)		
Lead (Pb)-free		IRFBF20STRLPbF ^a	IRFBF20STRRPbF ^a	IRFBF20LPbF		
Lead (FD)-free	b)-free SiHFBF20S-E3	SiHFBF20STL-E3 ^a	SiHFBF20STR-E3 ^a	SiHFBF20L-E3		
SnPb	IRFBF20S	IRFBF20STRL ^a	IRFBF20STRR ^a	IRFBF20L		
SHED	SiHFBF20S-E3	SiHFBF20STL ^a	SiHFBF20STR ^a	SiHFBF20L		

Note

a. See device orientation.

ABSOLUTE MAXIMUM RATI	NGS $T_C = 25 ^{\circ}C$, unless other	wise noted		
PARAMETER	SYMBOL	LIMIT	UNIT	
Drain-Source Voltage ^e		V _{DS}	900	v
Gate-Source Voltage ^e		V _{GS}	± 20	v
Continuous Drain Current	V_{GS} at 10 V $\frac{T_{C} = 25 \degree C}{T_{C} = 100 \degree C}$		1.7	
	V_{GS} at 10 V $T_C = 100 \text{ °C}$		1.1	А
Pulsed Drain Current ^{a,e}	I _{DM}	6.8		
Linear Derating Factor		0.43	W/°C	
Single Pulse Avalanche Energy ^{b, e}	E _{AS}	180	mJ	
Repetitive Avalanche Currenta	I _{AR}	1.7	A	
Repetitive Avalanche Energy ^a	E _{AR}	5.4	mJ	
Maniana David Dissignation	T _C = 25 °C	D	54	w
Maximum Power Dissipation	T _A = 25 °C	P _D	3.1	vv
Peak Diode Recovery dV/dtc, e	dV/dt	1.5	V/ns	

* Pb containing terminations are not RoHS compliant, exemptions may apply

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ABSOLUTE MAXIMUM RATINGS $T_C = 25 \degree C$, unless otherwise noted						
PARAMETER	SYMBOL	LIMIT	UNIT			
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to + 150	°C			
Soldering Recommendations (Peak Temperature)	for 10 s		300 ^d	U U		
Mounting Torque	6-32 or M3 screw		10	N		

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11). b. $V_{DD} = 50 \text{ V}$; starting $T_J = 25 \text{ °C}$, L = 117 mH, $R_G = 25 \Omega$, $I_{AS} = 1.7 \text{ A}$ (see fig. 12). c. $I_{SD} \le 1.7 \text{ A}$, dl/dt $\le 70 \text{ A/}\mu\text{s}$, $V_{DD} \le V_{DS}$, $T_J \le 150 \text{ °C}$. d. 1.6 mm from case.

e. Uses IRFBF20/SiHFBF20 data and test conditions.

THERMAL RESISTANCE RATINGS						
PARAMETER	RAMETER SYMBOL TYP. MAX. UN					
Maximum Junction-to-Ambient (PCB Mounted, steady-state) ^a	R _{thJA}	-	40	°C/W		
Maximum Junction-to-Case	R _{thJC}	-	2.3			

Note

a. When mounted on 1" square PCB (FR-4 or G-10 material).

SPECIFICATIONS $T_J = 25 \ ^{\circ}C$, unless other	wise noted					
PARAMETER	SYMBOL	TES	MIN.	TYP.	MAX.	UNIT	
Static					-		
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} -	= 0 V, I _D = 250 μA	900	-	-	V
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$	Reference	ce to 25 °C, I _D = 1 mA	-	1.1	-	mV/°C
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} =	= V _{GS} , I _D = 250 μA	2.0	-	4.0	V
Gate-Source Leakage	I _{GSS}		V _{GS} = ± 20 V	-	-	± 100	nA
Zara Cata Valtaga Drain Current		V _{DS} =	= 900 V, V _{GS} = 0 V	-	-	100	- μΑ
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 720 V	∕, V _{GS} = 0 V, T _J = 125 °C	-	-	500	
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 1.0 A ^b	-	-	8.0	Ω
Forward Transconductance	9 _{fs}	$V_{DS} = 50 \text{ V}, \text{ I}_{D} = 1.0 \text{ A}^{b}$		0.6	-	-	S
Dynamic							
Input Capacitance	C _{iss}		V _{GS} = 0 V,		490	-	pF
Output Capacitance	C _{oss}	$V_{DS} = 25 V,$		-	55	-	
Reverse Transfer Capacitance	C _{rss}	t = 1	.0 MHz, see fig. 5	-	18	-	1
Total Gate Charge	Qg		$I_{D} = 1.7 \text{ A}, V_{DS} = 360 \text{ V},$ see fig. 6 and 13 ^b	-	-	38	
Gate-Source Charge	Q _{gs}	V _{GS} = 10 V		-	-	4.7	nC
Gate-Drain Charge	Q _{gd}			-	-	21	
Turn-On Delay Time	t _{d(on)}	- V _{DD} = 450 V, I _D = 1.7 A,		-	8.0	-	
Rise Time	tr			-	21	-	
Turn-Off Delay Time	t _{d(off)}		$R_{\rm G} = 18 \ \Omega, \ V_{\rm GS} = 10 \ V, \ \rm see \ fig. \ 10^{\rm b}$		56	-	ns
Fall Time	t _f	1		-	32	-]



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SPECIFICATIONS $T_J = 25 \text{ °C}$, unless otherwise noted							
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	١ _S	MOSFET symbol showing the	-	-	1.7	А	
Pulsed Diode Forward Current ^a	I _{SM}	p - n junction diode	-	-	6.8	A	
Body Diode Voltage	V _{SD}	$T_J = 25 \ ^{\circ}C, \ I_S = 1.7 \ A, \ V_{GS} = 0 \ V^b$	-	-	1.5	V	
Body Diode Reverse Recovery Time	t _{rr}	T _J = 25 °C, I _F = 1.7 A, dl/dt = 100 A/µs ^b	-	350	530	ns	
Body Diode Reverse Recovery Charge	Q _{rr}	$I_{\rm J} = 25$ C, $I_{\rm F} = 1.7$ A, $dI/dt = 100$ A/µs ^o	-	0.85	1.3	μC	
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_{S} and $L_{\text{D}})$					

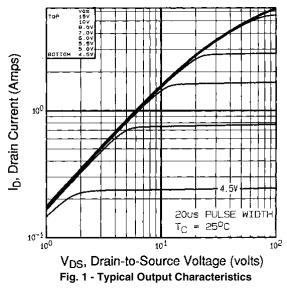
Notes

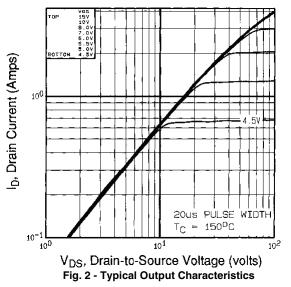
a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).

b. Pulse width \leq 300 µs; duty cycle \leq 2 %.

c. Uses IRFBF20/SiHFBF20 data and test conditions.

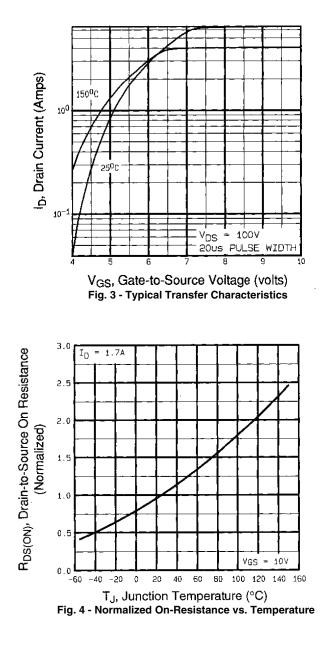


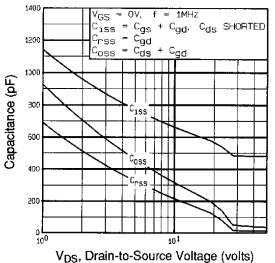


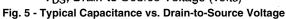


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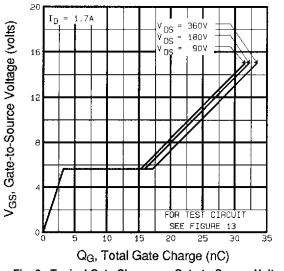


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage



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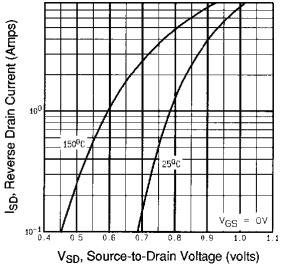
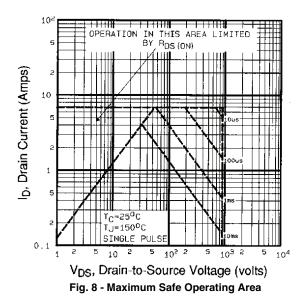


Fig. 7 - Typical Source-Drain Diode Forward Voltage



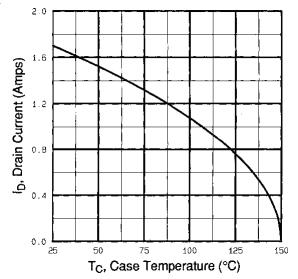


Fig. 9 - Maximum Drain Current vs. Case Temperature

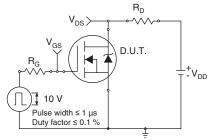


Fig. 10a - Switching Time Test Circuit

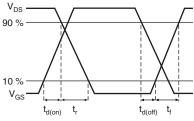
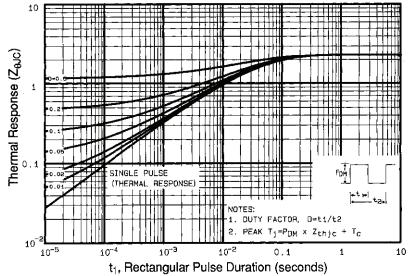
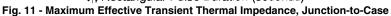


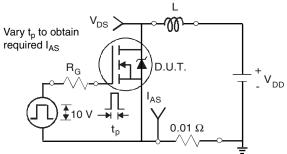
Fig. 10b - Switching Time Waveforms

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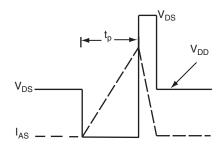


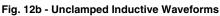


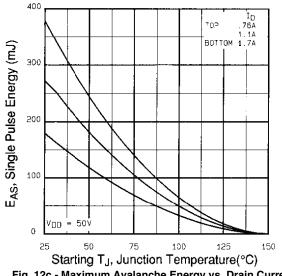














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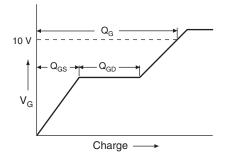


Fig. 13a - Basic Gate Charge Waveform

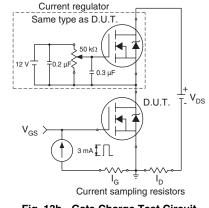


Fig. 13b - Gate Charge Test Circuit

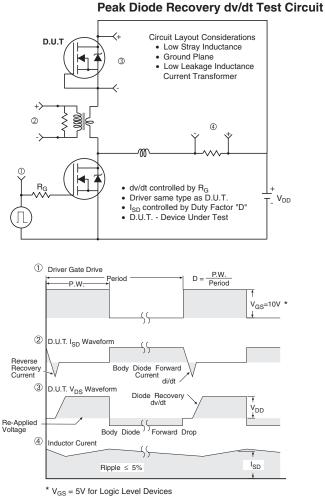


Fig. 14 - For N-Channel

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