## Features:

- Fully Compliant with OIF 99.102
- SONET/SDH Jitter Compliant
- High-speed Output Clock
- Narrow Clock-to-Data Skew Range
- Low Power 1.7W (Typ)
- +3.3V Single Supply
- Continuous Tuning Operation from 9.953 to 10.709Gb/s Rates
- 155-168/622-670 MHz Reference Clock Input
- Reliable 90-Ball BGA Package
- Up to 90°C Case Temperature

Specifications:

- 9.953 to 10.709Gb/s Continuous Operation
- Data Output Voltage Swing: 600 mV (Min)
- Data Output Rise/Fall: 25ps (Typ)
- 10ps Wideband Jitter (Max)
- High Speed Clock Voltage Swing: 600 MV (Min)
- +/- 15 ps Clock to Data Skew Range Over Temperature
- Supply Voltage: 3.3V (Typ)
- Total Power Dissipation: 1.7W (Typ)
- Operating Temperature Range: 0°C to +90°C (case)
- 15x15mm Low Profile 90 Ball TBGA (Taped BGA) Package
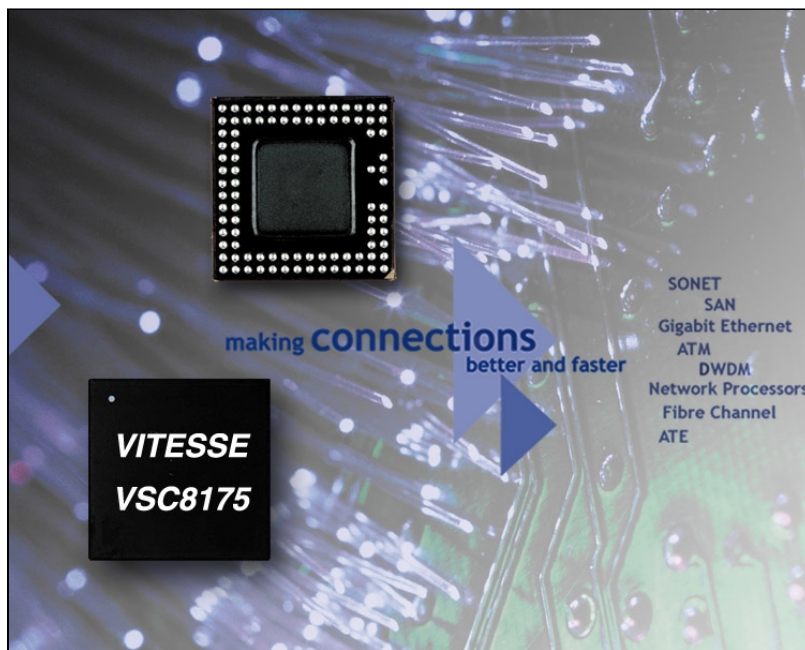
General Description

The VSC8175 consists of a 16:1 multiplexer and a clock generator for use in SONET STS-192/SDH STM-64 systems. The 16:1 multiplexer accepts 16 parallel LVDS inputs and PARITY at a data rate of 622.08Mb/s to 669.31Mb/s. This parallel data stream is then serialized into a 9.953Gb/s to 10.709Gb/s output. The clock generator creates the 9.953GHz to 10.709GHz clock signal used to re-time the transmitted serialized data. The clock generator requires a 155 to 167MHz or 622 to 669MHz PECL reference clock input. To ease timing constraints on the parallel interface, a 16-bit wide FIFO is included. A divided-by-16 or divide-by-64 LVDS clock output is available for use as a clock input to the parallel data source. Additional features include parity checking of a parity bit that is clocked in with the 16-bit parallel data, Bit Order Swap and Data Polarity Invert. To assist in monitoring device operation a Loss-of-Lock alarm and internal temperature sensing are provided. The device is packaged in a modified 90-Ball Grid Array (BGA).

Product Brief

Benefits:

- Provides High-speed Output Clock for RZ and Re-timed Laser Driver Applications

- Provides Lowest Power Solution in its Performance Class

- Pin-compatible Upgrade Paths to Lower Power Follow-on Solution (VSC8173LP) and Advance FEC (11.5 to 12.5Gb/s) Solutions (VSC8185)

- Integrated PLL Based Clock Generator

- Meets SONET/SDH Jitter Generation Requirements

- Compliant LVDS Interface

- Thermal Expansion of TBGA Package is Matched to the PC Board for High Reliability

- Input FIFO to Simplify Parallel Interface Timing

- Loss-of-Lock and Internal Temperature Sensing to Assist in Monitoring Device Operation

- Data Polarity Invert and Bit Order Swap for Ease of Layout

Applications:

- SONET/SDH Networking

- RZ Modulation

- Re-Timing Laser Drivers

- DWDM Systems

- G.975/709 Forward Error Correction (FEC)

- Ultra-Long Haul System

- Telecommunications Transmission Systems

- Test Equipment

VSC8175 Block Diagram
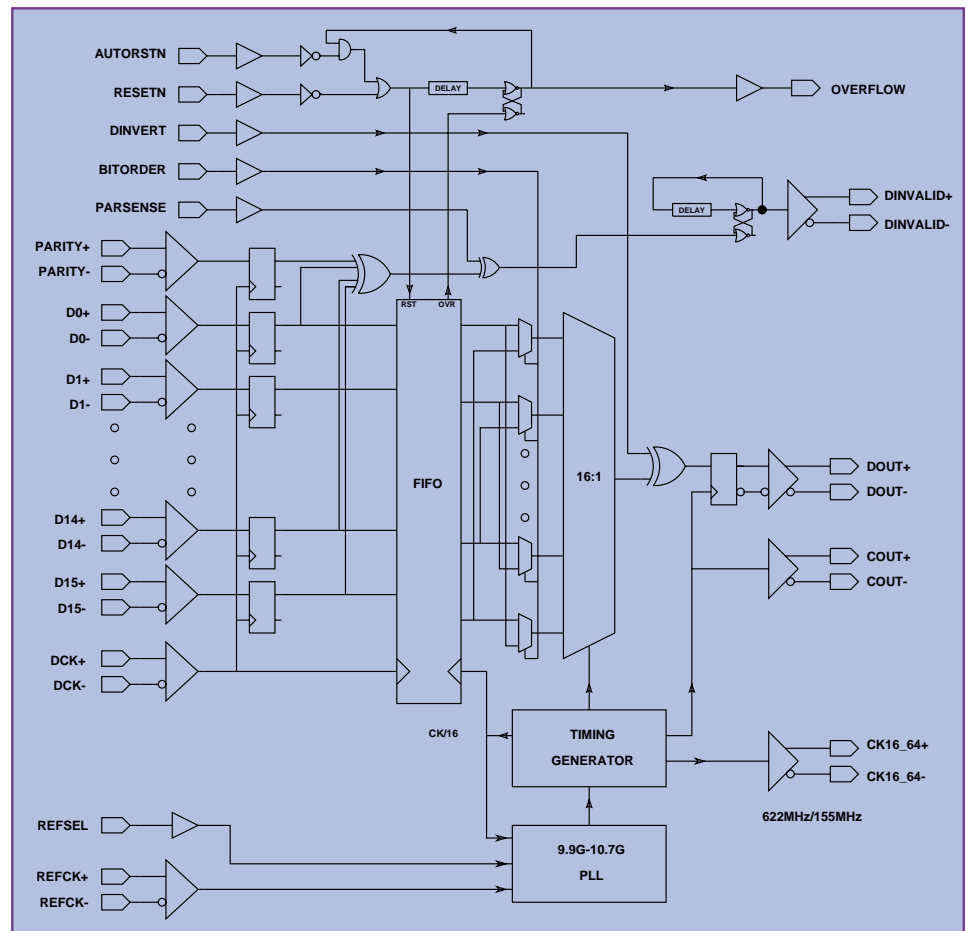
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